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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/865,564	05/29/2001	Jih-Shiang Jenq	NAUP0287USA	3996

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NAIPO (NORTH AMERICA INTERNATIONAL PATENT OFFICE)
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER
PHAM, LONG

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 06/28/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/865,564	Applicant(s) JENQ, JIH-SHIANG
	Examiner Long Pham	Art Unit 2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-13 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-8 is/are rejected.

7)☒ Claim(s) 9-13 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 3, 4, 5, 6, and 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in view of Yu (US '191), Arita et al. (US '304), Lehmann et al. (US '903), Ohmishi et al. (US '460), and Jung et al. (US '281).

AAPA teaches a method of forming a capacitor in a ferroelectric random access memory (FeRAM) on a semiconductor wafer, the semiconductor wafer comprising a substrate 12, and an insulation layer 14 positioned on the substrate, the method comprising (see figures 1-4 and the Description of the Prior Art on pages 1-5 of this application):

forming a bottom electrode 18 on the insulation layer;

forming a capacitor dielectric layer 22 on the surface of the dielectric layer; and forming an upper electrode 26 on the capacitor dielectric layer.

AAPA fails to teach that the capacitor dielectric layer and upper electrode are formed on the bottom electrode by a method in which a dielectric layer is formed over the substrate including the bottom electrode, the dielectric layer is etched to form a hole in the dielectric layer, spacers are formed on the sidewalls of the hole, and the capacitor layer and upper electrode are formed on the bottom electrode within the hole as recited in present claim 1.

Yu teaches a self-alignment contact technique in which a dielectric layer 26 is formed over a bottom conductor 21c, the dielectric layer is etched to form a hole 28 in the dielectric layer, spacers 29 are formed on the sidewalls of the hole, and a barrier layer 31 and a upper conductor 32 are formed on the bottom conductor within the hole. See figures 1-10 and col. 2, line 55 to col. 6, line 25.

It would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to a dielectric layer is formed over the substrate including the bottom electrode, etch the dielectric layer to form a hole in the dielectric layer, form spacers on the sidewalls of the hole, and form the capacitor layer and upper electrode on the bottom electrode within a hole in the method of AAPA because in doing so the undesired effects of leakage and shorts are reduced. See col. 1, lines 60-67.

AAPA fails to teach that the bottom electrode is made of platinum as recited in present claim 2.

However, it is well-known to ***one of ordinary skill in the art of making semiconductor devices*** that the bottom electrode of the capacitor of a memory device is made of platinum.

AAPA fails to teach that the capacitor dielectric layer is made of lead zirconate titanate (PZT) as recited in present claim 4.

However, it is well-known to ***one of ordinary skill in the art of making semiconductor devices*** that the capacitor dielectric layer is made of lead zirconate titanate (PZT).

AAPA fails to teach that the upper electrode is made of platinum as recited in present claim 8.

However, it is well-known to ***one of ordinary skill in the art of making semiconductor devices*** that the upper electrode of the capacitor of a memory device is made of platinum.

AAPA fails to teach that the bottom electrode is made of both a platinum layer and a titanium layer as recited in present claim 3.

Ariat teaches that a bottom electrode of a capacitor is made of both a platinum layer and a titanium layer. See col. 5, lines 20-25.

It would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to use both the platinum layer and titanium layer as the bottom electrode in the method of AAPA because in doing so a semiconductor device having capacitor with high reliability can be obtained. See col. 2, lines 45-50.

AAPA fails to teach that the dielectric layer is made of both a silicon dioxide layer and a titanium dioxide layer as recited in present claim 5.

Lehmann teaches that both silicon dioxide layer and titanium dioxide layer are used as dielectric material. See col. 2, lines 59-65.

It would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to use both silicon dioxide layer and titanium dioxide layer as dielectric material in the method of AAPA because the combination of silicon dioxide layer and titanium dioxide layer provides good insulation effect. See col. 2, lines 59-65.

AAPA fails to teach that the spacers are made of titanium dioxide as recited in present claim 6.

Ohmishi teaches that a spacer is made of titanium dioxide. See col. 8, lines 15-25.

It would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to use titanium dioxide as spacer material in the method of AAPA because in doing so the deterioration of the device ferroelectric characteristics are prevented. See col. 2, lines 50-52.

AAPA fails to teach that the upper electrode is made of iridium dioxide as recited in present claim 7.

Jung teaches that the upper electrode is made of iridium dioxide. See col. 7, lines 30-40.

It would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to use iridium dioxide as the upper electrode in the method of AAPA because in doing so reliable electrical contact between a buried contact plug and a lower electrode of the capacitor can be obtained. See col. 3, lines 10-15.

Allowable Subject Matter

3. Claims 9-13 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 703-308-1092. The examiner can normally be reached on M-F, 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-4082 for regular communications and 703-746-4082 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Long Pham
Primary Examiner
Art Unit 2823

L. P.

June 18, 2002